

Integrated Product and Process Control for Sustainable Semiconductor Manufacturing

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Abstract Semiconductor fabrication is a manufacturing sequence with hundreds of sophisticated unit operations and it is always challenged by strategy development for ensuring the yield of defect-free products. In this paper, an advanced control strategy through integrating product and process control is established. The proposed multiscale scheme contains three layers for coordinated equipment control, process control and product quality control. In the upper layer, online control performance assessment is applied to reduce the quality variation and maximize the overall product performance (OPP). It serves as supervisory control to update the recipe of the process controller in the middle layer. The process controller is designed as an exponentially weighted moving average (EWMA) run-to-run controller to reject disturbances, such as process shift, drift and tool worn out, that are exerted to the operation. The equipment in the process is individually controlled to maintain its optimal operational status and maximize the overall equipment effectiveness (OEE), based on the set point given by the process controller. The efficacy of the proposed integrated control scheme is demonstrated through case studies, where both the OPP (for product) and the OEE (for equipment) are enhanced.

Keywords semiconductor manufacturing, run-to-run control, integrated product and process control

1 INTRODUCTION

During the past two decades, sustained technology transitions have been made in semiconductor industry to keep pace with Moore's law. As a result, great control challenges [1] are emerging due to a shrinking feature size (0.32 μm or smaller) and an enlarging wafer diameter (300 mm or bigger). The quest of advanced control strategies becomes more important for sustainable semiconductor manufacturing [2].

Semiconductor manufacturing is composed of a serial of batch or semi-batch processes. Tight quality control (QC) is difficult to realize due to the lack of *in-situ* measurements, *i.e.* the product quality can only be sampled by post-process wafer tests. This type of quality control is necessary but inefficient because it “waits for” the occurrence of product quality problem [3]. In practice, when a quality problem is identified from a previous run, statistical process control (SPC) is then applied to the process to update the recipe of the future runs in order to prevent the re-occurrence of the same problem. This is the fundamental idea for semiconductor run-to-run (RtR) process control [4, 5]. Over the past 20 years, there is a substantial growth in literature existing on various RtR control schemes [6], including exponentially weighted moving average (EWMA) control [7, 8], double-EWMA control [9] and RtR-MPC control [10], *etc.*

However, most of the researches on RtR control assume that there is only one single product fabricated in a manufacturing line. This is far from reality in a modern semiconductor fab, which is characterized by the “mixed-product” nature, *i.e.*, products with different specifications can be fabricated on the same set of

equipments in a parallel way [11] as shown in Fig. 1.

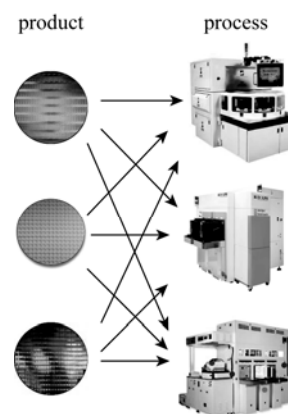


Figure 1 Semiconductor manufacturing with mixed-product nature

Such a high-mixed manufacturing mode leads to degradation in capacity as well as product quality. State estimation [12, 13] was therefore needed in order to implement RtR control in such a mixed-product manufacturing. However, the estimation is an approximation of the real process state, and in most cases one cannot distinguish the root cause of the shifted states. In such circumstance, even an elaborate RtR control strategy will fail though it may be perfect for one product. Process control alone may not have effect or even does harm to the overall product quality.

Recently, it is recognized that proactive product QC [14] must be coordinated with the process control, *i.e.* to integrate product and process control (IPPC) [3, 14]. This methodology would be an agreeable solution for

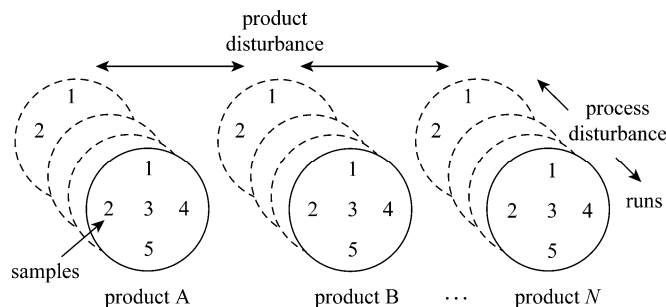


Figure 2 Multiple products manufactured in a sequence

the simultaneous control of products and batch semiconductor processes in a high-mixed manufacturing fab. In this paper, the philosophy of integrated product and process control is adopted and modified to catch up the real nature of semiconductor manufacturing.

2 CONTROL SCHEME

2.1 Theory development

From the product point of view, the main concern is the wafer product quality (film thickness and uniformity, etc.). In semiconductor manufacturing, the product output of each unit process can be described by a linear model.

$$Y_k = \alpha + \beta U_{k-1} + \eta_k \quad (1)$$

where α is the model bias from target and β is the input-output gain, Y_k is the measured quality characteristic of run k , U_{k-1} is the control action decided based on previous measurement Y_{k-1} , and η_k is the noise disturbance. It is usually represented by an IMA(1,1) time series model [4].

$$\eta_k = \eta_{k-1} + \delta + (1 - \theta z^{-1}) \varepsilon_k \quad 0 \leq \theta \leq 1 \quad (2)$$

where $\varepsilon_k \sim N(0, \sigma_\varepsilon^2)$ is a white noise sequence, and δ is the drift term, representing the tool aging effect exhibiting in many semiconductor processes. This effect could introduce deterministic drift disturbance and lead to severe quality variations.

Due to the lack of *in-situ* measurements, the product output can only be sampled through post-process wafer tests, *i.e.* the feedback is delayed for at least one run. Real-time process control is impossible for most of the unit operations. As a tradeoff, RtR control was proposed to control the current-run operation based on a previous-run feedback. The most used RtR control is the exponentially weighted moving average (EWMA) controller [7, 8], which serves as the bread and butter for semiconductor process control in the past two decades. The form of EWMA control is given below.

$$\begin{cases} Y_k = \alpha + \beta U_{k-1} + \eta_k \\ \gamma_k = \lambda(Y_k - bU_{k-1}) + (1 - \lambda)\gamma_{k-1} \\ U_k = (Y_r - \gamma_k) / b \end{cases} \quad (3)$$

where γ is the moving average of the model bias α ; b is a good estimation of β ; and λ is the EWMA controller gain (weighting factor). Supposing there is only one single product fabricated in the process, it is proved that EWMA control can achieve satisfactory performance as long as the drift term is not too big [15, 16]. However, in a mixed-product environment where multiple products are fabricated by the same process and equipment, the disturbance dynamics (δ , θ) differ from products, and the product performance could be largely degraded. Therefore, the EWMA gain (or recipe) λ should be adjusted for different products according to different disturbances.

Considering a mixed-product manufacturing as shown in Fig. 2, there are two types of disturbances, process disturbance between runs and product disturbance between products, which will cause quality variations.

According to time series analysis, the overall product performance (OPP) can be described by the long-run mean square error (MSE) of system output [17]

$$\text{MSE}(Y_k) = \text{Var}(Y_k) + \mu^2 = \sum_{j=1}^N [\text{Var}(Y_{k,j}) + \mu_j^2] \quad (4)$$

where μ_j is defined as mean deviation from target $Y_{r,j}$ (the specification of each product), *i.e.* $\mu_j = E[Y_{k,j}] - Y_{r,j}$. The objective of product control is to optimize the overall product performance. No matter which type of product is being manufactured, the quality variation would be reflected in Eq. (4) and the MSE value should be minimized to achieve a better product quality.

For a EWMA RtR controller, it is proved [15] that the overall control performance can be evaluated as below.

$$\text{MSE}(Y_{k,j}) = \underbrace{(1 + f_{1,j}^2 + \cdots + f_{d-1,j}^2)}_{\text{MVP}} \sigma_{\varepsilon,j}^2 + \frac{(1 - \lambda_j - \theta_j)^2}{1 - (1 - \lambda_j)^2} \sigma_{\varepsilon,j}^2 + \left(\frac{\delta_j}{\lambda_j} \right)^2 \quad (5)$$

The first term on the right hand side represents the minimum variance performance (MVP), the intrinsic feature of disturbances that is uncontrollable. To optimize the overall product performance, we have the optimization problem.

$$\min f(\lambda_j) = \frac{(1 - \lambda_j - \theta_j)^2}{1 - (1 - \lambda_j)^2} \sigma_{\varepsilon,j}^2 + \frac{\delta_j^2}{\lambda_j^2}$$

$$s.t. \quad 0 < \lambda_j < 1, \quad j = 1, \dots, N \quad (6)$$

where the parameters θ_j , δ_j , $\sigma_{\varepsilon,j}$ are the disturbance nature when the j th product is fabricated. Therefore, an optimal EWMA control gain (weighting factor) $\lambda_{j,\text{opt}}$ can be computed out as long as the disturbance natures θ_j , δ_j and $\sigma_{\varepsilon,j}$ are known. In this paper, $\lambda_{j,\text{opt}}$ represents the recipe for process controller.

2.2 On-line closed-loop identification

To implement the above approach, the parameters θ , δ , σ_ε should be known in advance. If there is only one single product in the manufacturing line, these parameters can be estimated by design of experiment (DOE) or regression analysis [18]. However, in a mixed-product manufacturing, dozens of products are fabricated in a semiconductor fab every day, and several products may only appear once. Therefore, it is impossible and unnecessary to estimate those parameters via off-line methods. An on-line identification approach will be much appreciated for the mixed-product manufacturing. The details about the approach are deduced as below.

The EWMA control law in Eq. (3) is re-written as below. Here, the notation ∇ is an abbreviation of $(1 - z^{-1})$.

$$\begin{cases} \nabla Y_k = \beta \nabla U_{k-1} + \nabla \eta_k \\ \nabla U_k = -\frac{\nabla \gamma_k}{b} = -\frac{\lambda Y_k}{b} \\ \nabla \eta_k = \delta + (1 - \theta z^{-1}) \varepsilon_k \end{cases} \quad (7)$$

The above equations are equal to

$$\nabla Y_k = -\frac{\beta \lambda}{b} Y_{k-1} + \nabla \eta_k \quad (8)$$

Since b is a good estimation of β in Eq. (3), it can be assumed $b \approx \beta$ to have the following expression.

$$[1 - (1 - \lambda)z^{-1}]Y_k = \delta + (1 - \theta z^{-1})\varepsilon_k \quad (9)$$

i.e.,

$$Y_k - \frac{\delta}{1 - (1 - \lambda)z^{-1}} = \frac{1 - \theta z^{-1}}{1 - (1 - \lambda)z^{-1}} \varepsilon_k \quad (10)$$

Hence, the mean deviation μ can be calculated as

$$\mu = E(Y_k) = E\left[\frac{\delta}{1 - (1 - \lambda)z^{-1}}\right] = \frac{\delta}{\lambda} \quad (11)$$

Let $\varphi = 1 - \lambda$ and substitute Eq. (11) into Eq. (10), we can get

$$(1 - \varphi z^{-1})(Y_k - \mu) = (1 - \theta z^{-1})\varepsilon_k \quad (12)$$

As long as the output data sequence $\langle Y \rangle$ is given, μ can be computed as the output mean value, i.e. $\hat{\mu} = \bar{Y}$. Then an ARMA (1,1) model can be fit to the $(Y_k - \hat{\mu})$ time series to identify $\hat{\varphi}$ and $\hat{\theta}$. According to Eq. (11),

$$\hat{\delta} = \hat{\mu} \hat{\lambda} = \hat{\mu}(1 - \hat{\varphi}) \quad (13)$$

So far, the parameters θ and δ are identified.

The parameter σ_ε can be easily identified by any MVP assessment method [19].

2.3 Integrated product and process control

Till now, the IPPC scheme can be implemented for mixed-product semiconductor manufacturing. The hierarchical diagram is depicted in Fig. 3.

(1) The proposed integrated control scheme contains three layers for coordinated equipment control, process control and product quality control.

(2) The upper layer aims at product quality control. The objective is to reject product disturbance and maximize the overall product performance.

(3) In the upper layer, on-line control performance

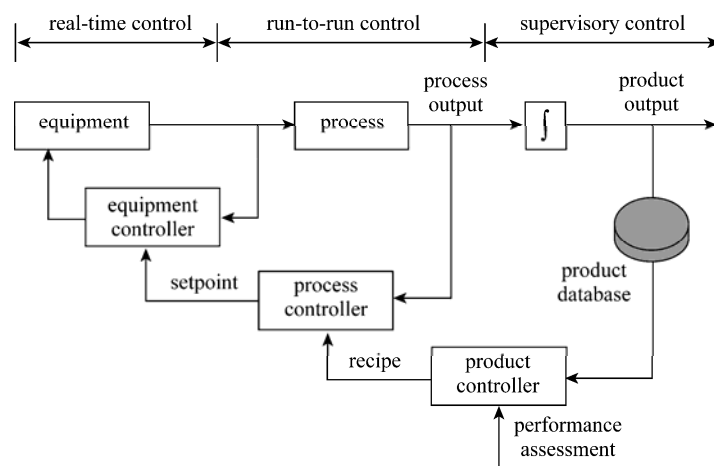


Figure 3 A multiscale scheme towards integrated process and product control

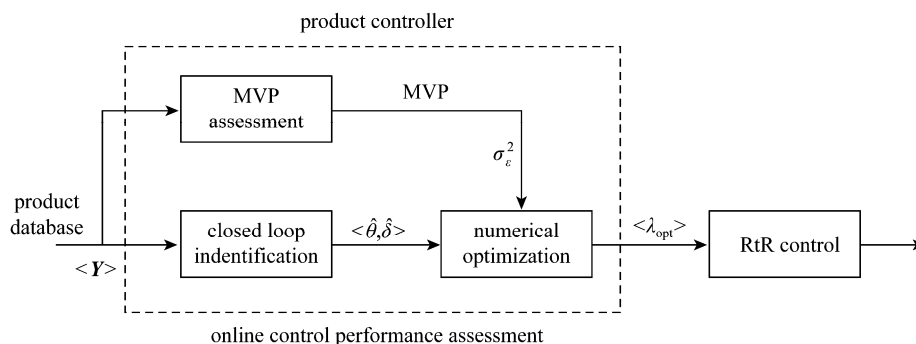


Figure 4 Conceptual design of the IPPC controller

assessment is carried out based on time series analysis of historical product data [20]. It serves as supervisory control and transfer the optimal recipe to the process controller in the middle layer.

(4) The middle layer aims at process control. The objective is to reject process disturbance and maximize the overall equipment effectiveness (OEE) [1].

(5) In the middle layer, due to the lack of *in-situ* sensors, the process controller is designed as an RtR-EWMA controller. The controller gain (weighting factor) is specified by the upper product control.

(6) The equipment layer aims to control operation conditions such as temperature, concentration and speed, *etc.*, of which the setpoints are given by the upper process controller. In practical, equipments are regarded as perfect controlled in real-time.

Thus, the integration of product (supervisory) control and process (RtR) control is realized. The details for the conceptual design of the IPPC controller are shown in Fig. 4. The only input is the routine output data $\langle Y \rangle$. This makes the IPPC approach easy to be performed and convenient to replace the existing RtR controllers.

3 CASE STUDIES

3.1 Chemical mechanical polishing

The chemical mechanical polishing (CMP) process is illustrated in this section to show the efficacy and attractiveness of the proposed IPPC scheme. The CMP developed by IBM in 1980s is known as a global surface planarization technology. It is regarded as one of the key unit operations in semiconductor manufacturing.

A typical diagram of CMP process is shown in Fig. 5. The wafer surface can be polished through the relative movement to the polishing pad. The slurry is distributed between wafer and polishing pad to generate chemical reactions, which will help removal of SiO_2 or copper at the surface.

A simulated CMP model in Eq. (14) developed by SEMATECH [4] is studied here. There are two SISO control loops in the CMP process. For loop 1, the product quality to be controlled is the within-wafer non-uniformity (y_1), and for loop 2 the controlled

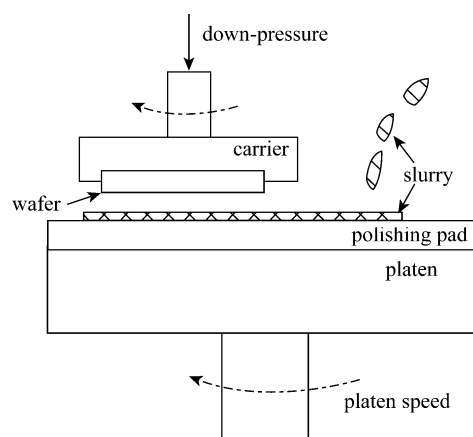


Figure 5 The diagram of CMP process

variable is the removal rate (y_2). The manipulated variables for loop 1 and loop 2 are the polishing down-pressure (u_1) and the platen speed (u_2), respectively.

$$\begin{cases} y_{1,k} = 254 + 32.6u_{1,k-1} + \frac{\delta_1}{1-z^{-1}} + \frac{1-\theta_1z^{-1}}{1-z^{-1}}\varepsilon_{1,k} \\ y_{2,k} = 1563.5 + 159.3u_{2,k-1} + \frac{\delta_2}{1-z^{-1}} + \frac{1-\theta_2z^{-1}}{1-z^{-1}}\varepsilon_{2,k} \end{cases} \quad (14)$$

It is known that control of CMP process is difficult because of poor understanding of the process, worn out of polishing pads, lacking of *in-situ* sensor, and mixed-product nature. Below, the power of IPPC philosophy will be demonstrated in case studies to overcome these difficulties.

3.2 Single product manufacturing

First, an easier manufacturing mode, *i.e.* the CMP only fabricates one single product is considered.

3.2.1 Process control only

Because the product qualities, *i.e.* removal rate and within-wafer non-uniformity can only be measured by post-process inspection, two EWMA-based RtR controllers [see Eq. (3)] are designed to control

both SISO loops. Supposing one product is being manufacturing, the characteristics of noise disturbance for loop 1 and loop 2 are described as below.

$$\eta_{1,k} = \eta_{1,k-1} - 0.6 + (1 - 0.65z^{-1})\varepsilon_{1,k} \quad (15)$$

$$\eta_{2,k} = \eta_{2,k-1} - 5.7 + (1 - 0.7z^{-1})\varepsilon_{2,k} \quad (16)$$

where $\varepsilon_{1,k} \sim N(0, 8^2)$, $\varepsilon_{2,k} \sim N(0, 10^2)$

Practical experience recognized that for a small drift process, the weighting factor of EWMA controller should be set between 0.1–0.3. In this study, we specify $\lambda_1 = \lambda_2 = 0.15$ for both SISO loops.

The overall product performance (OPP) index is defined as below

$$\text{OPP} = \frac{\text{MVP}}{\text{SYS}}, \quad \text{OPP} \in [0, 1] \quad (17)$$

where MVP stands for minimum variance performance, which is easy to derive by a control performance assessment method [19]; SYS stands for the real product performance [$\text{SYS} = \sum_{i=1}^{\text{RN}} y_i^2 / (\text{RN} - 1)$, RN, run number]. A larger OPP value is preferred. When $\text{OPP} = 1$, the CMP process is operated under best condition, *i.e.* minimum variance.

Thus, some insights for the process (RtR) control based CMP operation can be obtained. The results are summarized in Table 1.

Table 1 Overall product performance under RtR process control

	Recipe λ	Output offset	MVP	SYS	OPP
loop 1	0.15	-4.25	68.61	97.35	0.70
loop 2	0.15	-37.27	114.60	1562.67	0.07
loop 2	0.45	-12.55	108.34	264.89	0.41

Loop 1 has a smaller drift ($\delta = -0.6$), therefore a relative small weighting factor ($\lambda = 0.15$) is acceptable ($\text{OPP} = 0.7$). Loop 2 has a larger drift ($\delta = -5.7$), thus $\lambda = 0.15$ is no longer suitable (note: $\text{OPP} = 0.07$). Therefore, re-tuning the EWMA controller is needed. As given in Table 1 (the last line), $\text{OPP} = 0.41$ ensures a much better product quality when $\lambda = 0.45$.

3.2.2 Integrated product and process control

The proposed IPPC scheme is also applied to the above case study. First, a series of routine product data $\langle Y_1, Y_2 \rangle$ are collected. Time series analysis is then performed to identify the noise disturbance models, $\eta_{1,k} = \eta_{1,k-1} - 0.61 + (1 - 0.68z^{-1})\varepsilon_{1,k}$ and $\eta_{2,k} = \eta_{2,k-1} - 5.82 + (1 - 0.69z^{-1})\varepsilon_{2,k}$, which correspond well with the real noises [Eqs. (15, 16)]. Control performance assessment is then carried out base on Eqs. (5, 6). As a result, the optimal recipes for EWMA controllers are

updated, and the OPP index is improved. Detailed results are summarized in Table 2.

Table 2 Overall product performance under IPPC

	Updated recipe λ	Output offset	MVP	SYS	OPP
loop 1	0.40	-1.35	71.81	72.39	0.99
loop 2	0.82	-6.95	108.00	182.22	0.59

In a single product manufacturing environment, the main uncertainty is the process disturbance. The IPPC scheme can compensate the influence of disturbance and maximize the OPP index. For loop 2, unless change the EWMA controller into a double EWMA controller, the variance cannot be further reduced [15, 18].

3.3 Mixed-product manufacturing

The real nature of mixed-product semiconductor manufacturing is considered in this section. Supposing there are three products (A, B, C) fabricated in a sequence through CMP process, each product costs 300-run times. The accordant disturbance sequences are depicted in Fig. 6. Product A has a relatively smaller drift term. It could happen during the SiO₂ polishing to remove inter layer dielectric (ILD) between different levels of metallization. Products B and C have larger drift terms. They could happen during copper polishing.

3.3.1 Process control vs. IPPC

Below, the system performance by using process control (alone) and the coordinated IPPC is compared. For simplicity, only the control of within-wafer non-uniformity (*i.e.* control loop 1) is considered here.

$$y_{1,k} = 254 + 32.6u_{1,k-1} + \frac{\delta_1}{1 - z^{-1}} + \frac{1 - \theta_1 z^{-1}}{1 - z^{-1}} \varepsilon_{1,k} \quad (18)$$

The EWMA process control starts from product A using a tuned weighting factor ($\lambda = 0.05$). As shown in Fig. 7, the OPP for product A is quite satisfactory. However, when the products B and C enter the manufacturing line, the OPPs are fast degraded to 0.1–0.2. As expected, the product qualities will have large offsets from targets (see Fig. 8, run 300–900). The reason is that copper is harder than ILD materials, leading to a larger drift in disturbance. As analyzed in the previous section, larger weighting factors should be used for these products.

The IPPC also starts from product A with $\lambda = 0.05$. The difference is that IPPC can update the weighting factor (recipe) automatically for each product in every run. This is benefited from the on-line identification and on-line performance assessment. The moving window technology is used to generate a time series of 50-run length. The disturbance characteristics are then identified and transferred to the performance assessment program, which updates the recipe of EWMA in

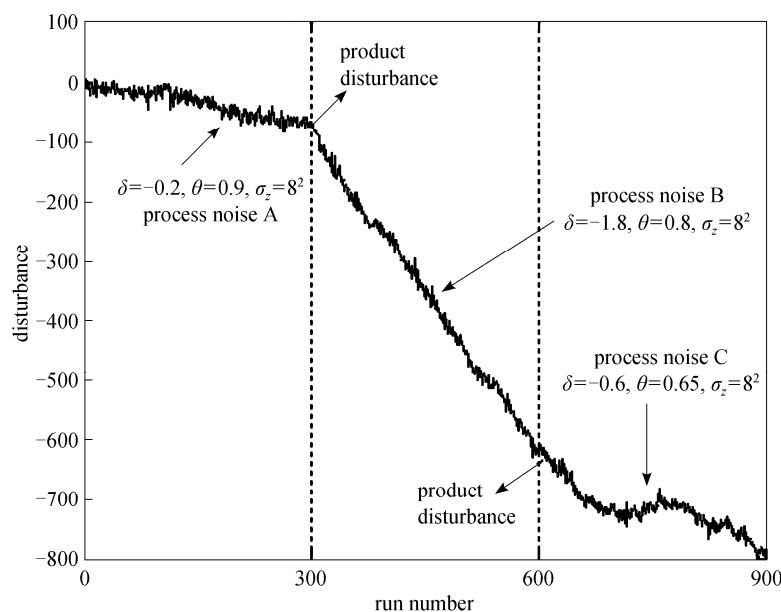


Figure 6 Disturbance dynamics in a mixed-product manufacturing

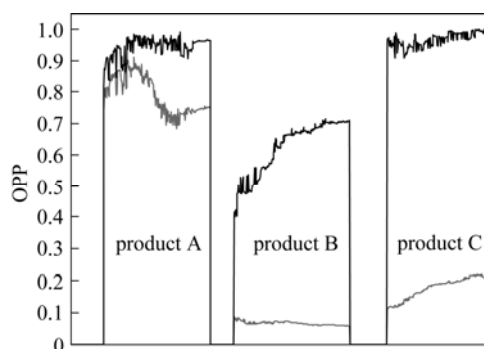
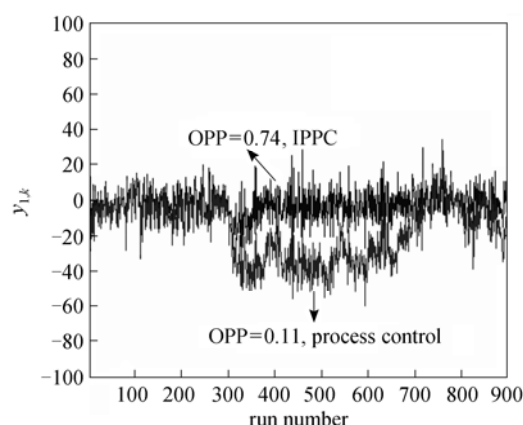
Figure 7 Comparison of process control (only) and IPPC in a mixed-product manufacturing
— process control; — IPPC

Figure 8 Product outputs under process control (only) and IPPC

the process control layer.

The OPPs by using IPPC are depicted in Fig. 7. Products A and C can be perfectly controlled to achieve minimum variance performance and the OPP for product B is also acceptable. For the manufacturing sequence of all A, B, C products, IPPC ensures a high OPP about 0.74, while process control alone (with $OPP=0.11$) is obviously not suitable to control a mixed-product manufacturing.

The quest for sustainability in semiconductor lies in many aspects. On the product side, one needs to control quality on target to ensure defect-free products and to maximize the overall product performance (OPP) index.

On the process side, one needs to improve the overall equipment efficiency (OEE). In a CMP process, the lifetime of a polishing pad is quite limited due to the wear out effect. The study on IPPC links process

layer with the equipment layer. The down-pressure and the platen speed could be adjusted to prevent over-polishing, thus to increase the life time of polishing pad. Moreover, the IPPC scheme reduces the use of test wafers, which can accelerate the fabrication and improve OEE.

Because the unit operations in semiconductor manufacturing are usually described by a linear model as shown in Eqs. (1, 2), the proposed IPPC scheme is a general and effective approach for most of the key unit operations such as chemical vapor deposition (CVD), plasma etching, film deposition, rapid thermal processing (RTP), and lithography, etc.

4 CONCLUSIONS

The manufacturing of semiconductor is known as

very sophisticated, and it is always challenged by strategy development for ensuring the yield of defect-free product as well as process efficiency. An advanced multiscale approach towards integrated product and process control (IPPC) is proposed to tackle the sophisticated nature of the mixed-product semiconductor manufacturing. Case studies on the CMP operations show that the IPPC scheme can improve both the OPP for product quality and the OEE for process efficiency. Future studies on this topic will extend the IPPC philosophy to consider the environmental benefits in semiconductor manufacturing.

NOMENCLATURE

b	estimated input-output gain
U	manipulated variable
Y	product output
α	model bias from target
β	input-output gain
γ	moving average of model bias
δ	disturbance drift term
ε	white noise
η	disturbance
λ	weighting factor of EWMA control
μ	mean derivation
σ	variance

Subscripts

j	product index
k	run number
r	setpoint

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